Real-Time 28 Gb/s NRZ over 80 km SSMF in C-band using Analog Electronic Precompensation

M. Verplaetse, L. Breyne, J. Lambrecht, X. Yin, P. Ossieur, G.Torfs

IDLab, INTEC, Ghent University - imec, 9052 Ghent, Belgium

E-mail: michiel.verplaetse@ugent.be

Abstract: We demonstrate real-time C-band transmission of direct detected 28Gb/s NRZ/OOK over 80km SSMF using a Dual-Drive MZM and custom-designed SiGe BiCMOS 5-tap analog FIR filters to compensate chromatic dispersion without digital signal processing.

OCIS codes: (200.4650) Optical Interconnects; (060.2360) Fiber optics links and subsystems

1. Introduction

Direct detection (DD) receivers, used commonly nowadays, are not likely to lose interest in the near future. Although coherent schemes are used for inter data center applications and recent coherent-lite schemes [1] are trying to make their way into the datacenter interconnects, the added power dissipation, area and complexity could still swing the balance towards direct detection receivers. To do so, the transmission distance and data rate for DD links should be increased. Bandwidth limiting components and chromatic dispersion (CD) are two important parts that limit the DD performance. Equalization in the analog or digital domain should be employed to alleviate these issues. Due to the square law direct detection, equalization at the receiver is more difficult and less effective. Therefore, in the past, transmit-side precompensation using IQ Mach-Zehnder modulators (IQ-MZMs) [2, 3] or a single dual-drive MZM (DD-MZM) [4] was proposed to compensate for chromatic dispersion in the fiber. With the possibility to directly manipulate the complex electric field in the fiber, transmission over 300 km at 112 Gb/s is achieved in [3] using digital signal processing (DSP). An example architecture using a DD-MZM could look like the system in Fig. 1a making use of a CMOS DSP-core and necessary SiGe (or other technology) drivers. By independently driving both arms of the MZM with a filtered version of the input, compensation of the chromatic dispersion can be performed. Although very powerful, the DSP solutions introduce extra complexity, power and latency, which makes them less competitive compared to the coherent solutions that assume DSP as well. Therefore, it would be beneficial to perform the precompensation in the analog domain as proposed in [5] (using an IQ-MZM), leading to lower complexity, power and latency. In this paper, a single DD-MZM is used in combination with two on-chip analog finite impulse response (FIR) filters as shown in Fig. 1b. Fig. 1 compares the DSP-based implementation of such precompensation with a single (e.g. BiCMOS) chip solution. This last solution eliminates the need for a complex CMOS chip that includes demultiplexing (DSP can only be performed at a reduced clock rate of no more than a few GHz), DSP, two digital-to-analog converters (DACs) and the required clock generation blocks (phase locked loops, PLLs). In addition, the power hungry 50 Ω high-speed interface between the CMOS chip and SiGe BiCMOS driver can be eliminated.

The amount of chromatic dispersion that can be compensated will be limited by the physical length of the FIR filters. In this paper we use two analog 5-tap FIR filters to perform the compensation for 28 Gb/s NRZ/OOK signals generated by an FPGA. These allow us to demonstrate real-time transmission at 1550 nm below the KP4-FEC threshold up to 70 km SSMF and below the 7%-OH HD-FEC threshold up to 80 km SSMF. As no compensation of the CD for 28 Gb/s NRZ/OOK leads to a sub-FEC transmission limit of only 20 km in C-band [5], an increase in distance with a factor four is accomplished. As a result, we cover a broad range for inter datacenter applications using direct detection without using any form of DSP (apart from the need of FEC, which can be done on the host devices) as all filtering is performed in the analog domain.

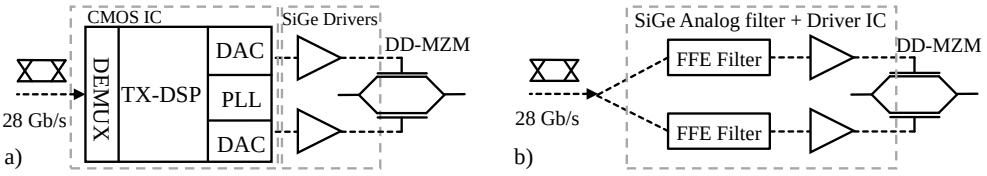


Fig. 1. Precompensation system of a single DD-MZM using (a) a DSP approach, (b) analog filtering. (DAC = digital-to-analog converter; PLL = phase locked loop to generate high-speed clocks)

2. Experimental Setup and Optimization

To evaluate the analog precompensation principle, the setup shown in Fig. 2 is used. Using the high speed transceiver on an FPGA, a 28 Gb/s NRZ pseudo random bit sequence (PRBS) test pattern with a length of $2^{31}-1$ is generated. The output driver of the FPGA comprises a pre- and post cursor allowing to precompensate electrical losses. This signal is then filtered by two independently tunable, integrated distributed analog 5 tap FIR filters (shown in Fig. 2d) with a tap spacing of 27 ps and sufficient bandwidth to handle 28 Gbaud signals [5]. These filters are part of an analog IC implementing 4 filters, schematically shown in Fig. 2c, and designed in a 55nm BiCMOS technology. The core power consumption of 2 filters is approximately 100 mW. The outputs of the IC are amplified by 14 dB using external amplifiers to drive the separate arms of a DD-MZM ($LiNbO_3$, V_π =3.5 V). A 1550 nm continuous wave laser with 13 dBm of output power is coupled to the modulator. When biased at quadrature, around 3 dBm of optical power is launched into a SSMF and around 7.2 dB of extinction is obtained. At the receiver a photodiode (PD) (responsivity = 0.8 A/W) and 55nm BiCMOS TIA [6] are used to convert the optical signal to the electrical domain. The light is guided towards the PD via a fiber probe and a C-band grating coupler. To compensate for the grating coupler loss and to allow evaluation of the CD tolerance of the system for long fibers with extensive loss, an EDFA is introduced. The lowest power into the EDFA was -16.4dBm, hence the OSNR was sufficiently high that no optical filtering was necessary to eliminate BER degradation due to ASE noise. A variable optical attenuator (VOA) is added to control the input power on the PD. The TIA output signal is sent either to a high-speed sampling scope (DSO) to observe the final eye diagrams, a real-time oscilloscope (RTO) to perform the equalizer optimization or to a BER tester for real-time BER measurements.

The transfer function of both FIR filters can be controlled by changing the gain of on-chip analog amplifiers (5 for each filter, a_0 through a_4), visible in Fig. 2d. These gains can be set using a serial peripheral interface (SPI). After direct detection, the optical phase information is lost. Hence optimization of the filter tap settings is challenging for various amounts of CD. To this end, an iterative update procedure that can optimize this nonlinear system is used. We vary the setting of each independent amplifier with a fixed (small) step size and capture the corresponding waveforms in the RTO. By comparing these waveforms with a reference waveform, we can locally linearize the system and iteratively optimize the coefficients based on the Gauss–Newton algorithm.

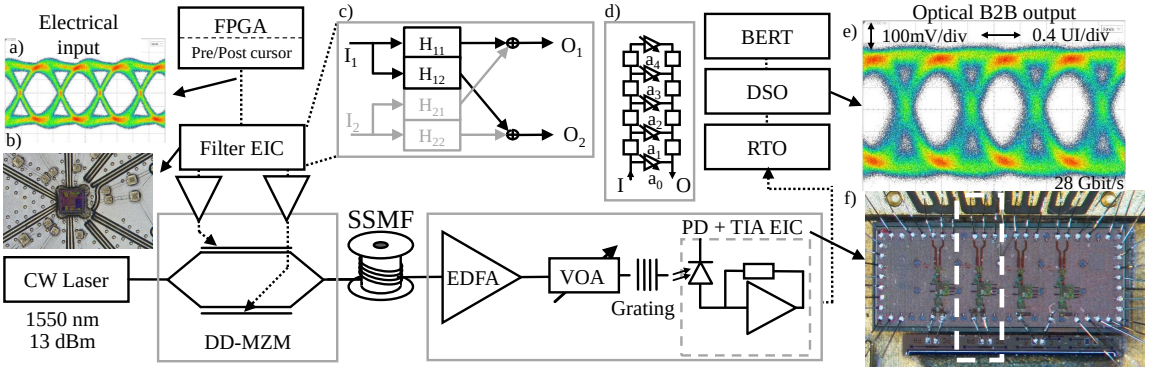


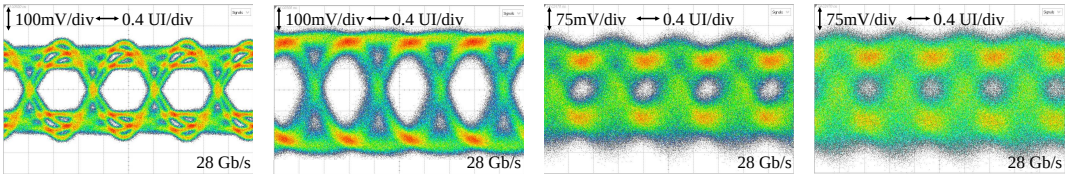
Fig. 2. Overview of the experiment setup. (a) The electrical eye diagram at FPGA output without precompensation. (b) Analog filter IC on the PCB. (c) Flow graph of the filter IC. (d) Distributed implementation of a FIR filter. (e) Optical B2B receive eye diagram. (f) Photo of the TIA+PD ICs.

3. Results and Discussion

Using the setup and the optimization principle discussed in the previous section, transmission experiments over different fiber spans are performed. First a fixed (but limited) amount of pre- and post cursor peaking is introduced via the analog predistortion of the FPGA. This peaking helps to compensate bandwidth losses in the cables towards the IC. By this means, both analog filters have to introduce less peaking (common to both) and can use their limited amount of taps more effectively to compensate the CD. The fixed precompensated eye output from the FPGA transceivers is shown in Fig. 3a. For each fiber length, the output of the TIA is first connected to the RTO to perform the optimization of the filter coefficients. During each optimization, the received optical power on the photodiode was equal to -6.5 dBm (controlled by the VOA). After the iterative optimization, the output is connected to the BERT to observe the BER in real-time. While observing the BER, minor manual adjustments are performed to the filter tap settings to compensate for the differences in analog response between the RTO and the BERT. The different eye diagrams of these final settings at -6.5 dBm average optical power, captured by the DSO, are found in Fig. 3b to Fig. 3d. As expected,

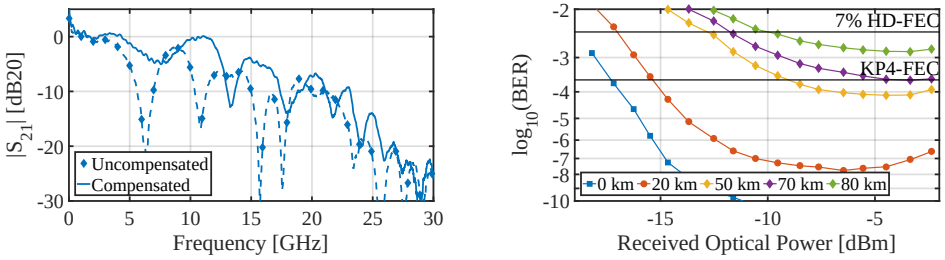
with increasing distance, the eyes start to close and the output swing decreases due to the transmit-side filtering. By varying the VOA attenuation in the system, BER curves can be measured for all transmission experiments. The results are found in Fig. 4b, together with the annotation of two commonly used FEC limits (7%-OH HD FEC=3.8e-3,KP-4 FEC = 2.4e-4). All BER curves show an error floor and even curl back up in function of the received optical power. This is caused by the TIA which enters the nonlinear regime. The transmission range can be extended up to 80 km below the HD-FEC limit and up to 70 km below the KP4-FEC limit. If no compensation of the CD for would be applied, transmission in C-band is limited to maximally 20 km as the created spectral notch is very close to the Nyquist frequency of 14 GHz [5]. This means that an increase in distance with a factor four is accomplished using the analog FIR filters with a limited length of 5 taps. Increasing the filter length would lead to further extension of this distance.

To show the influence of the filter, the small signal response of the optical link at 80 km of SSMF with and without the compensation is measured and shown in Fig. 4a. The response is measured from the input of the filters to the output of the TIA, hence, the introduced peaking in the FPGA is not present. It is clear that without the compensation, several notches (lowest around 6.4 GHz) caused by the chromatic dispersion are present. Turning on the compensation shows that the notches are shifted to higher frequencies allowing to accomplish the transmission over 80 km of fiber.



(a) FPGA output (b) 0 km (c) 70 km (d) 80 km

Fig. 3. The precompensated eye diagram measured at the output of the FPGA (a) and the eye diagrams at the output of the optical links for the experiments over different lengths of SSMF (b)-(d).



(a) (b)

Fig. 4. (a) Small signal response of the 80 km optical link with and without compensation (from input filter IC to output TIA). (b) BER curves in function of the incident power on the PD.

4. Conclusion

By using analog pre-compensation filters and a dual-drive MZM, we demonstrated 28 Gb/s NRZ/OOK transmission up to 80km SSMF with a direct detection receiver. The proposed direct detection link makes use of two independent analog 5-tap FIR filters driving two arms of a DD-MZM to compensate the present chromatic dispersion in the C-band. Compared to common solutions using DSP precompensation, a low complexity and lower power solution can be obtained. Using 28 Gb/s data directly generated from an FPGA, transmission of a PRBS31 stream over 80 km of SSMF is demonstrated under the 7%-OH HD FEC ($\leq$3.8e-3).

Acknowledgment

We thank the ERC Advanced Grant 695495 (ATTO), the Special Research Fund and the Research Foundation Flanders.

5. References

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